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On Design of a Fault Tolerant Reversible 4-Bit Binary Counter with Parallel Load

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Abstract: Reversible logic is one of the ways for power optimization. The produced circuits using these gates are applied in nanotechnology, bioinformatics, quantum computing and DNA. In this paper, we propose a fault tolerant reversible 4-Bit binary counter with parallel load. This is a robust and first attempt for designing a fault tolerant reversible 4-Bit binary counter with parallel load. Counters are important components in computers. Most counters are synchronous in computer systems. Some of these counters can also be made from D-Flip Flops. Counters can be designed to generate any desired sequence of states. The sequence may follow the binary count or may be any other arbitrary sequence. In this study, we propose three approaches of the fault tolerant reversible circuits for 4-Bit binary counter with parallel load. Total logical calculation and Total quantum cost of the second approach is less than the previous approaches. Third approach is implemented using Unit 3 gate. The constant inputs and the garbage outputs of its circuit is less than the mentioned approaches. All the scales are in the nanometric area. The proposed circuits can be applied for constructing more complex systems in nanotechnology.

Key words: Reversible Logic Circuit, Fault Tolerant Reversible Counter, Reversible Binary Counter, Nanometric Counter, Quantum Computing

INTRODUCTION

One of the major purposes in the hardware design is low power circuit design. Conventional circuit design causes energy dissipation. The dissipation an amount of KTIn2 joules of energy is summarized as losing of each one bit, where $K=1.3806505*10^{-23}$ $m^2kgs^{-2}K^{-1}$ (joule/kelvin) is the Boltzmann's constant and T is the absolute temperature at which computation is performed (Landauer R., 1961; Vasudevan D. P. *et al*., 2004; Hayes B., 2006; Parhami B., 2006). In 1973, Bennett demonstrated that the reversible logic is the important factor for avoiding the KTIn2 energy dissipation (Hayes B., 2006; Bennett C. H., 1973). The reversible logic has applications in optical computing, DNA computing, quantum computing, low power CMOS design and nanotechnology. In reversible circuit synthesis, Fan-out is not allowed (Vasudevan D. P. *et al*., 2004; Perkowski M., 2001; Perkowski M and P Kerntopf, 2001).

Traditional gates like AND, NAND, OR do not have reversible features. The specific features of the traditional gates are different with the reversible logic gates. In the last years, some of the reversible synthesis ways are suggested (P. Gupta, *et al*., 2006; D. Maslov, 2005). One of the ways for optimal synthesis of Reversible Logic circuits is the evolutionary computation approach (M. Lukac, *et al*., 2003). Standard Genetic Algorithm (GA) applied in this approach. Also, it discusses about new operators and optimization processes in the reversible logic circuits. Full Adders and multipliers are two important circuits in the arithmetic operations that are required to implement by quantum circuit logic. Some of the approaches are discussed about these circuits (M. Haghparast and K. Navi, 2007; M. Haghparast, *et al*., 2009).

Process of running the system both forward and backward can be implemented with reversible circuit logic. That is, the inputs can be generated from the outputs. However, stop and go back to any point of computation history is possible in reversible circuit logic. There are important features that should be used in reversible circuit synthesis. Some of these features are considered as:

- Minimum number of constant inputs
- Minimum number of garbage outputs
- Minimum number of reversible gates

Some of the outputs are called as garbage outputs that are not used for subsequent computations in the reversible circuit (H. Thapliyal and M. B. Srinivas, 2005; D. Maslov and G. W. Dueck, 2003). However, some of the inputs are named as constant inputs. These inputs are appended to an $n \times k$ equation for making it to a reversible circuit (S. Islam and R. Islam, 2005).

Quantum computing theory is basis of the quantum gates. The quantum circuits are reversible, because a restricted quantum mechanical system is reversible naturally. The 1×1 and 2×2 quantum gates are produced using some several quantum methods (P. Kaye, *et al*., 2007). Some of the gates like the 3×3 gates can not be generated using quantum technology straightly. This logic is a major reason for generating the bigger gates

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using the 1×1 and 2×2 gates. The quantum cost (QC) of a reversible circuit is the number of 1×1 and 2×2 gates in the quantum circuits. The QC is a main factor for evaluating a quantum circuit design (P. Gupta, *et al*., 2006). Low consumption traditional computing and quantum computing is required to the reversible calculating logic (A. De Vos, 2010).

Digital electronics is categorized into sequential logic and combinational logic. Combinational logic output depends on the inputs levels, whereas sequential logic output depends on stored levels and also the input levels. Synchronous and Asynchronous sequential circuits are two types of sequential logic circuits. Their classification depends on the timing of their signals. Asynchronous sequential circuit is a system whose outputs depend upon the order in which its input variables change and can be affected at any instant of time. Synchronous sequential circuit uses storage elements called flip-flops that are employed to affect their binary value only at discrete instants of time. Synchronous sequential circuits use logic gates and flip-flop storage devices. They have a clock signal as one of their inputs. All state transitions in such circuits occur only when the clock value is either 0 or 1 or happen at the rising or falling edges of the clock depending on the type of memory elements used in the circuit. Some of the approaches are discuss about design of the sequential circuits by quantum reversible logic (H. Thapliyal and N. Ranganathan, 2010; M. L. Chuang and C. Y. Wang, 2008).

A fault tolerant system is capable to working the operations appropriately. This property is beneficial when the failure is appeared in some of the system components. The failures in some of the fault tolerant systems can be detected and corrected easily (M. S. Islam, *et al*., 2009; M. S. Islam and Z. Begum, 2008; M. S. Islam *et al*., 2009). There is some of the error correcting codes (ECC) for correcting the failures in circuits. Hamming code is one of the important and useful codes and makes single-error-correcting and double-error-detecting (SEC-DEC) codes (R. K. James, *et al*., 2007). The fault tolerant full adder circuits are implemented by reversible logic circuit. These approaches have minimum number of garbage outputs and constant inputs. Also, the novel realization of fault tolerant reversible full adder circuit are presented in recently years (M. Haghparast and K. Navi, 2008 M. S. Islam *et al*., 2010).

One common requirement in digital circuits is counting, both forward and backward. A simple counter can be used to count pulses. All counters require a "square wave" clock signal to make their count. There are two major types of counter: ripple and synchronous. In simple circuits, their behaviour appears almost identical, but their internal structure is very different. A ripple counter contains a chain of flip-flops with the output of each one feeding the input of the next. When the input is changed from high to low (on the falling-edge), then the output changes state. This simple arrangement works well, but there is a slight delay as the effect of the clock "ripples" through the chain of flip-flops (H. Thapliyal and N. Ranganathan, 2010). A synchronous counter has a more complex internal structure to ensure that all its outputs are changed precisely together on each clock pulse, avoiding the brief false counts which occur with ripple counters. Counter circuits can be implemented by reversible logic circuit (M. Haghparast and M. Samadi Gharajeh, 2011).

Counters with parallel load can have a preset value. Load signal indicates that data should be loaded into the counter and clear signal resets counter to all zeros. Carry output signal could be used for higher-order bits. The 4-Bit counter with parallel load can be used to make a BCD counter using the load and clear inputs. A 4-Bit counter with getting inputs has a load signal that data can be loaded into the counter. A simple schematic of this counter is shown in fig. 1.

A 4-Bit counter with clear input has a clear signal that resets counter to all zeros. A simple schematic of this counter is shown in fig. 2.

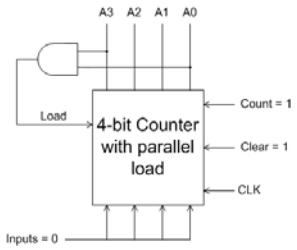

Fig. 1: 4-Bit Counter with Load Input

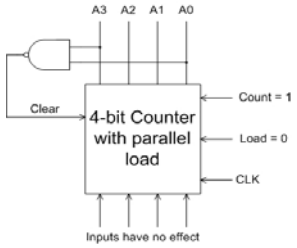

Fig. 2: 4-Bit Counter with Clear Input

In this paper, we propose three approaches of new fault tolerant reversible circuit for a 4-Bit binary counter that loads data as parallel state. First approach and second approach have minimum number of reversible gates and Total quantum cost. Total logic calculation of second approach is lesser than first approach, because it is designed using Unit 2 gate and Total logical calculation of Unit 2 is lesser than Unit 1. Third approach has better design than the mentioned approaches. It has minimum number of constant inputs and garbage outputs.

Background

Reversible logic:

Reversible logic circuits can be implemented by low power CMOS design. That is, they have minimum quantum cost for implementing the arithmetic operations. This is an important factor in the circuit design technology. Benefits of the reversible logic can be demonstrated in the implemented reversible logic gates in past years. This section describes the structure and operation of reversible gates that are applied in our circuits. However, we try that compare some of the reversible gates with other proposed circuits.

In additional study, we will describe the features of the quantum gates. A one-to-one correlation between the inputs and the outputs is a required factor for making an n-input n-output function F as a reversible state. That is, the output vector can be received from the input vector and the input vector can be achieved by the output vector.

Reversible logic gates:

An overview of the $n \times n$ reversible gate can be explained as:

$I_v = (I_1, I_2, I_{3,\ldots}, I_n)$
$O_v = (O_1, O_2, O_{3,\ldots}, O_n)$

Where I_v and O_v are specially input and output vectors. In the last years, some of the reversible logic gates have been proposed (M. Haghparast and K. Navi, 2008; R. Feynman, 1985; T. Toffoli, 1980; E. Fredkin and T. Toffoli, 1982; A. Peres, 1985; M. H. A. Khan, 2002; M. S. Islam, 2009; M. S. Islam and Z. Begum, 2008; M. S. Islam *et al*., 2009; H. Thapliyal and N. Ranganathan, 2010; M. Haghparast and K. Navi, 2008) such as: Feynman gate (FG) (R. Feynman, 1985), Toffoli gate (TG) (T. Toffoli, 1980), Fredkin gate (FRG) (E. Fredkin and T. Toffoli, 1982), Peres gate (PG) (A. Peres, 1985), New gate (NG) (M. H. A. Khan, 2002), HNG (M. Haghparast and K. Navi, 2008) and Feynman Double gate (F2G) (H. Thapliyal and N. Ranganathan, 2010; M. Haghparast and K. Navi, 2008).

Feynman gate (FG): Feynman gate is called as controlled-not gate (CNOT). This gate is a 2×2 reversible gate and can be represented as:

$I_v = (A, B)$
$O_v = (P = A, Q = A \oplus B)$

In above equations, I_v and O_v are input and output vectors sequentially. Nevertheless, "A" is control bit and "B" is the target bit. This gate can be applied for structuring fan-out values. That is, when B is '0' then the output bits (P, Q) are equal to A. In addition, it can be used as a not operation gate. That is, when A is '1' then one of the target output bits (Q) is NOT of B. Fan-out is not allowed in reversible logic circuit. Thus, Feynman gate is used to copy an input signal and put them in output bits. This gate has QC of one. The functionality of Feynman gate is displayed in Fig. 3.

Toffoli gate (TG): Toffoli gate is a 3×3 reversible gate. This gate is also known as controlled controlled-NOT (CCNOT). The Toffoli gate is also represented as:

$I_v = (A, B, C)$

$O_v = (P = A, Q = B, R = AB \oplus C)$

In mentioned equations, I_v is input vector and O_v is output vector. The Toffoli gate is a universal gate. That is, other reversible circuits can be designed by Toffoli gate. This gate also can be applied as AND gate. In fact, if input bit "C" is '0', then target output bit "R" is $A \times B$. Toffoli gate is implemented using five quantum 3×3 gates. Thus, the QC of this gate is five. An overview of Toffoli gate is shown in Fig. 4.

Fredkin gate (FRG): Fredkin gate is a 3×3 reversible gate. This gate is also presented as controlled permutation gate. It also can be described as:

$I_v = (A, B, C)$
$O_v = (P = A, Q = A'B \oplus AC, R = A'C \oplus AB)$

In above equations, I_v and O_v are input and output vectors sequentially. It is also known as a conservative gate. That is, the Hamming weight of its input and output vectors are equal together. The QC of this gate is five. A schematic of Fredkin gate and its functionality is shown in Fig. 5.

Peres gate (PG): Peres gate is a 3×3 reversible logic gate. It is implemented using one Toffoli gate and one Feynman gate. It is also known as New Toffoli gate (NTG). This gate can be explained as:

$I_v = (A, B, C)$
$O_v = (P = A, Q = A \oplus B, R = AB \oplus C)$

Where I_v and O_v are the input and output vectors. The symbol of Peres gate is shown in Fig. 6. The transformation generated by a Toffoli gate followed by a Feynman gate is equal to Peres gate. It is a universal gate and more complex than the Toffoli gate.

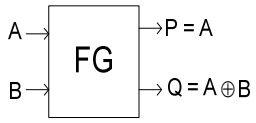

Fig. 3: Feynman gate

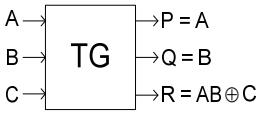

Fig. 4: Toffoli gate

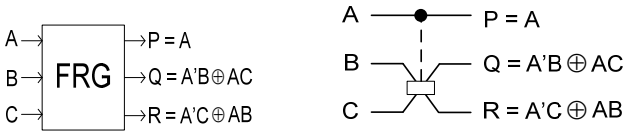

Fig. 5: Symbol and functionality of Fredkin gate

New gate (NG): New gate is a 3×3 reversible logic gate. This gate has QC of 7. The Peres gate can be explained as:

$I_v = (A, B, C)$
$O_v = (P = A, Q = AB \oplus C, R = A'C' \oplus B')$

Where I_v is input vector and O_v is output vector. However, it can also used as AND operation in the reversible circuits. When C is '0' then one of the output bits (Q) is AND computation of A and B. The New gate is shown in Fig. 7.

HNG gate: HNG gate is a 4×4 reversible logic gate. The QC of the HNG gate is six. This gate can be represented as:

I_v = (A, B, C, D)
O_v = (P = A, Q = B, R = A ⊕ B ⊕ C, S = (A ⊕ B).C ⊕ AB ⊕ D)

In mentioned equations, I_v and O_v are input and output vectors orderly. HNG gate is a universal gate. Full Adder circuit can be implemented using HNG gate. The Full Adder circuits using HNG gate have minimum number of QC. Thus, we can use them in the addition operations. The HNG gate is depicted in Fig. 8.

Feynman Double gate (F2G): Feynman Double gate is a 3×3 reversible logic gate. This gate is designed based on the Feynman gate, unless the Feynman gate has one control input bit, but the F2G gate has an extra input bit and one more output bit. This gate can be represented as:

I_v = (A, B, C)
O_v = (P = A, Q = A ⊕ B, R = A ⊕ C)

In above equations, I_v and O_v are the input and output vectors orderly. The symbol and functionality of F2G gate is shown in Fig. 9. It is a parity-preserving reversible logic gate.

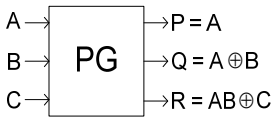

Fig. 6: Peres gate

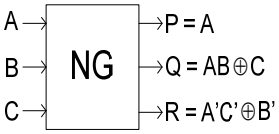

Fig. 7: New gate

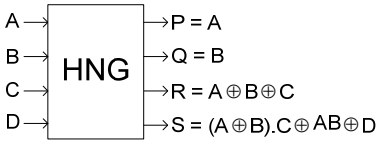

Fig. 8: HNG gate

3. Our Proposed Quantum Realization of Parity Preserving Reversible Unit 1:

Unit 1 is a 8×8 fault tolerant reversible logic gate. The parity preserving logic is one the major features of this gate. This gate produces AB and A ⊕ B output expressions. We will use these functions in our approaches. This gate is designed of three F2G gate and one FRG gate. It has QC of 11. This gate can be explained as:

I_v = (A, B, C, D, E, F, G, H)
O_v = (P = A, Q = A ⊕ B, R = A ⊕ C, S = ((A ⊕ C)'.D) ⊕ ((A ⊕ C).E),
T = ((A ⊕ C)'.E) ⊕ ((A ⊕ C).D), U = D ⊕ F, V = A ⊕ C ⊕ D ⊕ G, W = A ⊕ C ⊕ H)

In above equations, I_v is input vector and O_v is output vector. Any fault is not allowed that affects more than a single signal readily detectable at the elementary outputs of designed circuit. It is also a universal gate. Unit 1 and its output expressions are depicted in Fig. 10. Implementing of the AND, XOR operations in same circuit is the important goal to design this unit. We can design these operations by FRG, F2G gates, but the produced circuit will have much reversible gate with more constant inputs and garbage outputs. Thus, we decide to design these operations in the same circuit that has low constant input bits and garbage output bits. That is, this gate is an optimal reversible circuit and has also the fault tolerant features.

4. Our Proposed Quantum Conception of Parity Preserving Unit 2:

Unit 2 is a 5×5 fault tolerant reversible logic gate. This gate produces AND, XOR functions in the fault tolerant reversible circuits. It has QC of 7. Truth table of this gate is shown in Table 1. This gate can be explained as:

I_v = (A, B, C, D, E)
O_v = (P = A, Q = A'B ⊕ AC, R = A'C ⊕ AB, S = (A'C ⊕ AB) ⊕ D, T = (A'C ⊕ AB) ⊕ E)

Fig. 9: Symbol of Feynman Double gate and its functionality

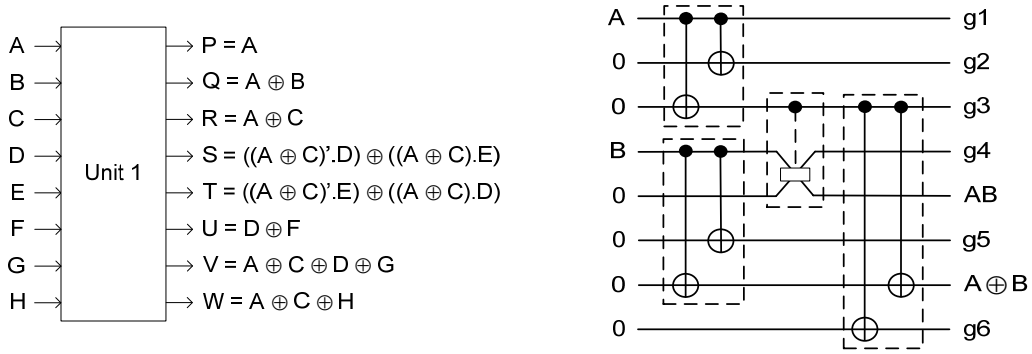

Fig. 10: Our proposed equivalent quantum representation of parity preserving reversible Unit 1

In mentioned equations, I_v and O_v are input and output vectors orderly. Unit 2 is a universal gate. That is, it can be used in some of the reversible circuits. Symbol and functionality of its circuit is shown in Fig. 11. We can design AB ⊕ C output by some reversible gates like FRG gate, but it will have much reversible gate and very complexity circuit and have also more constant inputs and garbage outputs. This cause to realize of the produced circuit become very difficult and it will have much value of quantum cost. Therefore, we decide to design and implement this output in the same circuit that has low constant input bits and garbage output bits. That is, this gate is an optimal reversible circuit and has also the fault tolerant features.

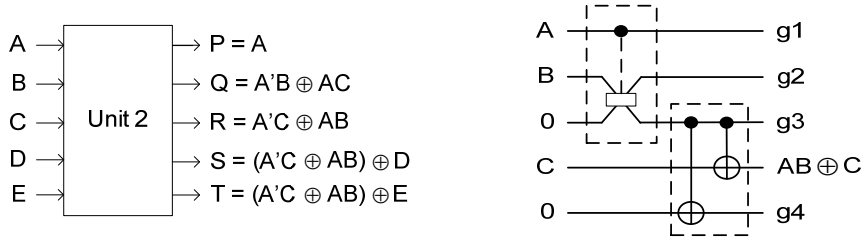

Fig. 11: Quantum representation of our proposed parity preserving reversible Unit 2

Table 1: Truth table of Unit 2 gate

A	B	C	D	E	P	Q	R	S	T
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	1	1
0	0	1	0	1	0	0	1	1	0
0	0	1	1	0	0	0	1	0	1
0	0	1	1	1	0	0	1	0	0
0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	1	0	0	1
0	1	0	1	0	0	1	0	1	0
0	1	0	1	1	0	1	0	1	1

0	1	1	0	0	0	1	1	1	1
0	1	1	0	1	0	1	1	1	0
0	1	1	1	0	0	1	1	0	1
0	1	1	1	1	0	1	1	0	0
1	0	0	0	0	1	0	0	0	0
1	0	0	0	1	1	0	0	0	1
1	0	0	1	0	1	0	0	1	0
1	0	0	1	1	1	0	0	1	1
1	0	1	0	0	1	1	0	0	0
1	0	1	0	1	1	1	0	0	1
1	0	1	1	0	1	1	0	1	0
1	0	1	1	1	1	1	0	1	1
1	1	0	0	0	1	0	1	1	1
1	1	0	0	1	1	0	1	1	0
1	1	0	1	0	1	0	1	0	1
1	1	0	1	1	1	0	1	0	0
1	1	1	0	0	1	1	1	1	1
1	1	1	0	1	1	1	1	1	0
1	1	1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1	0	0

5. Our Proposed Fault Tolerant Reversible Unit 3:

Parity preservation is a fault tolerant feature in the reversible circuits. All of the gates should be parity preserving to making a fault tolerant characteristic for reversible circuits. In this section, we propose a new quantum equivalent circuit of parity preserving Unit 3. It produces the required expressions in output bits. We are applied Unit 3 in our approaches for constructing the required fault tolerant circuits. Our approaches have XOR, AND operations. Thus, Unit 3 makes these operations in the mentioned circuits. Symbol and functionality of the proposed circuit is shown in Fig. 12.

Unit 3 is a 4×4 reversible logic gate that construct the parity preserving reversible circuits. It is a parity preserving logic circuit. That is, parity of the inputs is equal to parity of the outputs. It can be used to any Boolean function. This is a fault tolerant reversible gate. The QC of this gate is seven. Truth table of this gate is shown in Table 2. Unit 3 can be represented as:

$I_v = (A, B, C, D)$

$O_v = (P = A, Q = A \oplus B, R = AB \oplus C, S = BD \oplus B'(A \oplus D))$

Where I_v and O_v are input and output vectors sequentially. This gate is one-through, which means one of the input bits is also output bit.

In this gate, the P output bit is same with A input bit. The Q output bit makes the XOR operations of the reversible circuits. The existence of the quantum V and V^+ gates cause to the latter output bits (R and S). These input bits can not straightly be produced in stage of the input bits. We can determine the R and S outputs by writing their truth table. For example when ABCD input bits are 1010, from left to right, the status of the V and V^+ gates on C to R path, and D to S path, are as:

Detail of the C to R path (Left to Right) is as:

1. In C to R path, V gate is passive because its control bit (B) is '0'.
2. In C to R path, V^+ gate is active because its control bit ($B \oplus A$) is '1'.
3. In C to R path, V gate is active because its control bit (A) is '1'.

There is a V*V=NOT operation in the C to R path that results to R = '1'. From above expressions, we can conclude that $R = AB \oplus C = 0 \oplus 1 = 1$.

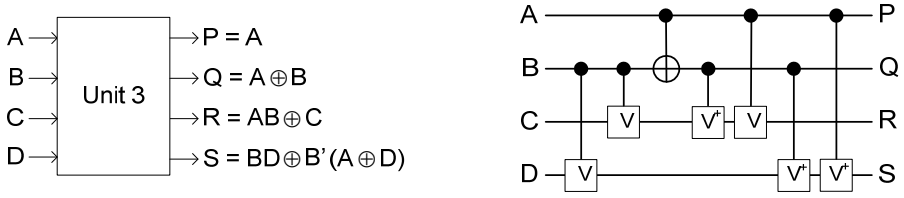

Fig. 12: Our proposed quantum representation of parity preserving reversible Unit 3

Table 2: Truth table of Unit 3 gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	1	0	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	1

Detail of the D to S path (Left to Right) is as:

1. In D to S path, V gate is passive because its control bit (B) is '0'.
2. In D to S path, V^+ gate is active because its control bit ($B \oplus A$) is '1'.
3. In D to S path, V^+ gate is active because its control bit (A) is '1'.

There is a $V*V^+=I$ operation in the D to S path that concludes to S = '1'. From above description, we can summarize that $S = BD \oplus D'.(A \oplus D) = 0 \oplus 1.(1 \oplus 0) = 0 \oplus 1 = 1$.

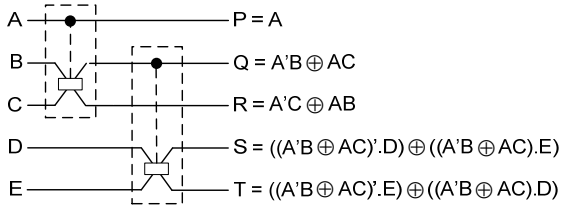

Fig. 13: Quantum representation of our proposed parity preserving reversible Unit 4

Table 3: Truth table of Unit 4 gate

A	B	C	D	E	P	Q	R	S	T
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	1	1	0
0	0	1	1	1	0	0	1	1	1
0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	1	0	1	0
0	1	0	1	0	0	1	0	0	1
0	1	0	1	1	0	1	0	1	1
0	1	1	0	0	0	1	1	0	0
0	1	1	0	1	0	1	1	1	0
0	1	1	1	0	0	1	1	0	1
0	1	1	1	1	0	1	1	1	1
1	0	0	0	0	1	0	0	0	0
1	0	0	0	1	1	0	0	0	1
1	0	0	1	0	1	0	0	1	0
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1	0	1	0	1	1	1	0	1	0
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1	1	0	1	1	1	0	1	1	1
1	1	1	0	0	1	1	1	0	0
1	1	1	0	1	1	1	1	1	0
1	1	1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1

6. Our Proposed Quantum Conception of Parity Preserving Unit 4:

Unit 4 is a 5×5 fault tolerant reversible logic gate. This gate is composite of two FRG gate. It has QC of 10. It would be applied in our proposed D-Flip Flop circuit. Truth table of this gate is shown in Table 3. This gate can be explained as:

$I_v = (A, B, C, D, E)$
$O_v = (P = A, Q = A'B \oplus AC, R = A'C \oplus AB, S = ((A'B \oplus AC)'.D) \oplus ((A'B \oplus AC).E),$
$T = ((A'B \oplus AC)'.E) \oplus ((A'B \oplus AC).D))$

In mentioned equations, I_v and O_v are input and output vectors orderly. Unit 4 is a universal gate. That is, it can be used in some of the reversible circuits. The functionality of its circuit is shown in Fig. 13. The proposed circuit in this unit has fault tolerant feature. We decide to design an optimal circuit that has low constant inputs and garbage outputs. The internal circuit of D-Flip Flop gate has clock pulse input. Thus, we determine to implement this sequential circuit in a specific way that has true logical output with low reversible gate. The proposed circuit is not also very sophisticated schematic. This cause to final counter circuit has not unclear state. Also, this gate is an optimal reversible circuit and has also the fault tolerant features.

7. Our Proposed Circuit of Fault Tolerant Reversible D-Flip Flop:

The fault tolerant reversible D-Flip Flop is designed of our proposed Unit 4 Circuit. This gate produces the needed output expressions in our approaches. It could be used to design the complex sequential circuits in the future. This gate is a fault tolerant reversible D-Flip Flop circuit. We are called this gate as D-FF gate. The symbol and output expressions of its circuit are shown in Fig. 14.

The main equation of the D-FF gate can be written as $Q^* = DE + E'Q$. It is produced by internal circuit of the Unit 4 gate. Our proposed D-FF circuit has parity preserving feature. Thus, our design of the D-Flip Flop is a fault tolerant state. The proposed D-FF gate has optimized in the number of constant inputs, garbage outputs and reversible gates. Nevertheless, CP is clock pulse in the circuit. The internal circuit of the D-FF gate has '0' and '1' constant inputs that we are condoned from displaying them in our approaches circuits. The D-FF gate does not have a "No Change" condition. Thus, the feedback junction from output to input is essentially. Our proposed D-FF circuit has QC of 10.

8. 4-Bit Binary Counter with Parallel Load:

One common requirement in digital circuits is counting, both forward and backward. In the 4-Bit counter to the right, we are using edge-triggered master-slave flip-flops similar to those in the Sequential portion of these pages. The output of each flip-flop changes state on the falling edge (1-to-0 transaction) of the input bits. Binary counters with parallel load can be used to design different modulo-n counters. The 4-Bit binary counter is a circuit that goes through a prescribed series of states. The discussed 4-Bit parallel load counter in this lesson can be used to design any counter of modulo-n where $2 \leq n \leq 16$. The functionality of this counter is represented in Table 4. Counter signal is shown as "C" Pin that due to count next binary state. Load signal is shown as "L" Pin. If Load is asserted data, then inputs are loaded. In this circuit, Count input increments on each negative edge if negative edge triggered D-Flip Flops are used. The capabilities and functionality of its circuit are shown in Fig. 15. The circuit of this counter is composite of the four sections that perform the required computing. Each section has an output bit is called "Z" bit. It transfers the value of computing amount to next section.

The equations of the mentioned counter are explained as:

$Z_0 = L'.C$
$Q_0 = (Z_0 \oplus Q_0) + (L.D_0)$
$Z_1 = Z_0.Q_0$
$Q_1 = (Z_1 \oplus Q_1) + (L.D_1)$
$Z_2 = Z_1.Q_1$
$Q_2 = (Z_2 \oplus Q_2) + (L.D_2)$
$Z_3 = Z_2.Q_2$
$Q_3 = (Z_3 \oplus Q_3) + (L.D_3)$
$C_{out} = Z_3.Q_3$

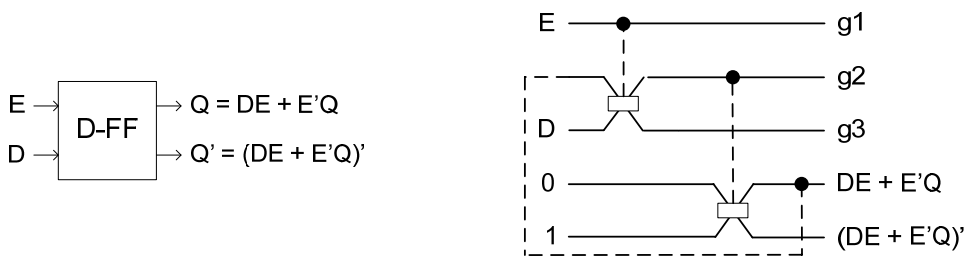


Fig. 14: Symbol and output expressions of D-FF gate

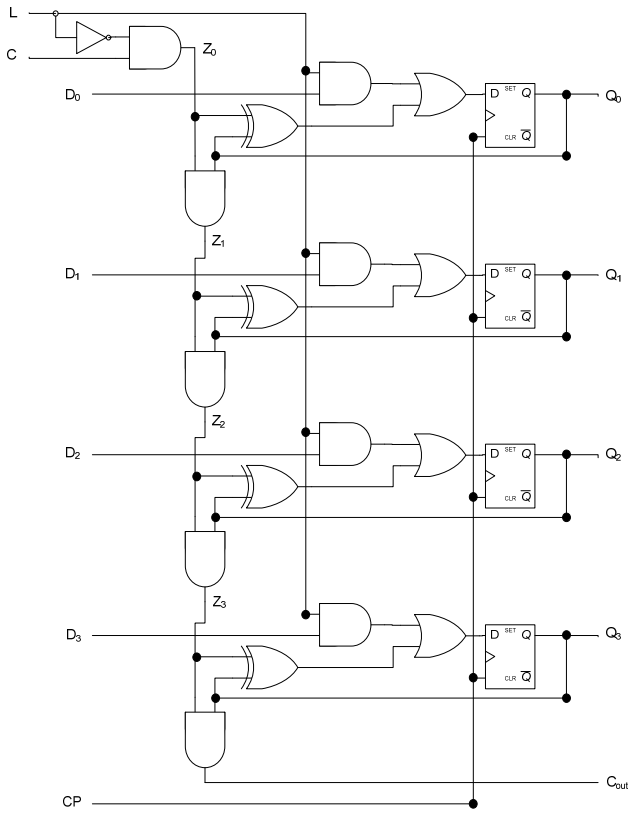


Fig. 15: 4-Bit Binary Counter with Parallel Load

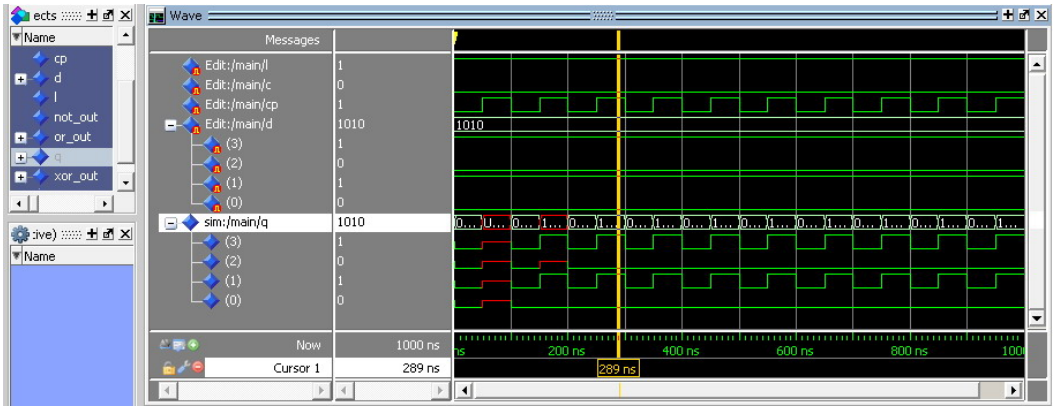
We have implemented circuit of this counter using VHDL top level language. VHDL code and its output simulation are shown in Fig. 16. Our main purpose of the design and implement this simulation is realizing of the traditional 4-Bit binary counter be very easy. This VHDL code has four sections. Every section exports a value into output bits that make the final outputs of the counter. In fact, traditional circuit of this counter is classified into four sections. This VHDL code is not related to our proposed approaches. But, it can be very benefit in delineation of 4-Bit binary counter with parallel load.

Table 4: Functionality of 4-Bit Binary Counter with Parallel Load

CLK	L	C	Function
↑	0	0	No Change
↑	0	1	Count Next Binary State
↑	1	0	Load Inputs

```
process (CP) is
begin
   Not_Out <= not L;
   Z_Out(0) <= Not_Out and C;

   -- Section 1
   AND_Out(0) <= L and D(0);
   XOR_Out(0) <= Z_Out(0) xor Q(0);
   OR_Out(0)  <= AND_Out(0) or XOR_Out(0);
   D_FF_0:    D_FF port map (OR_Out(0), CP, Q(0));
   Z_Out(1)   <= Z_Out(0) and Q(0);

   -- Section 2
   AND_Out(1) <= L and D(1);
   XOR_Out(1) <= Z_Out(1) xor Q(1);
   OR_Out(1)  <= AND_Out(1) or XOR_Out(1);
   D_FF_1:    D_FF port map (OR_Out(1), CP, Q(1));
   Z_Out(2)   <= Z_Out(1) and Q(1);

   -- Section 3
   AND_Out(2) <= L and D(2);
   XOR_Out(2) <= Z_Out(2) xor Q(2);
   OR_Out(2)  <= AND_Out(2) or XOR_Out(2);
   D_FF_2:    D_FF port map (OR_Out(2), CP, Q(2));
   Z_Out(3)   <= Z_Out(2) and Q(2);

   -- Section 4
   AND_Out(3) <= L and D(3);
   XOR_Out(3) <= Z_Out(3) xor Q(3);
   OR_Out(3)  <= AND_Out(3) or XOR_Out(3);
   D_FF_3:    D_FF port map (OR_Out(3), CP, Q(3));
   C_out      <= Z_Out(3) and Q(3);
end process;
```

(a)



(b)

Fig. 16: (a) VHDL code, (b) output simulation of 4-Bit binary counter with parallel load

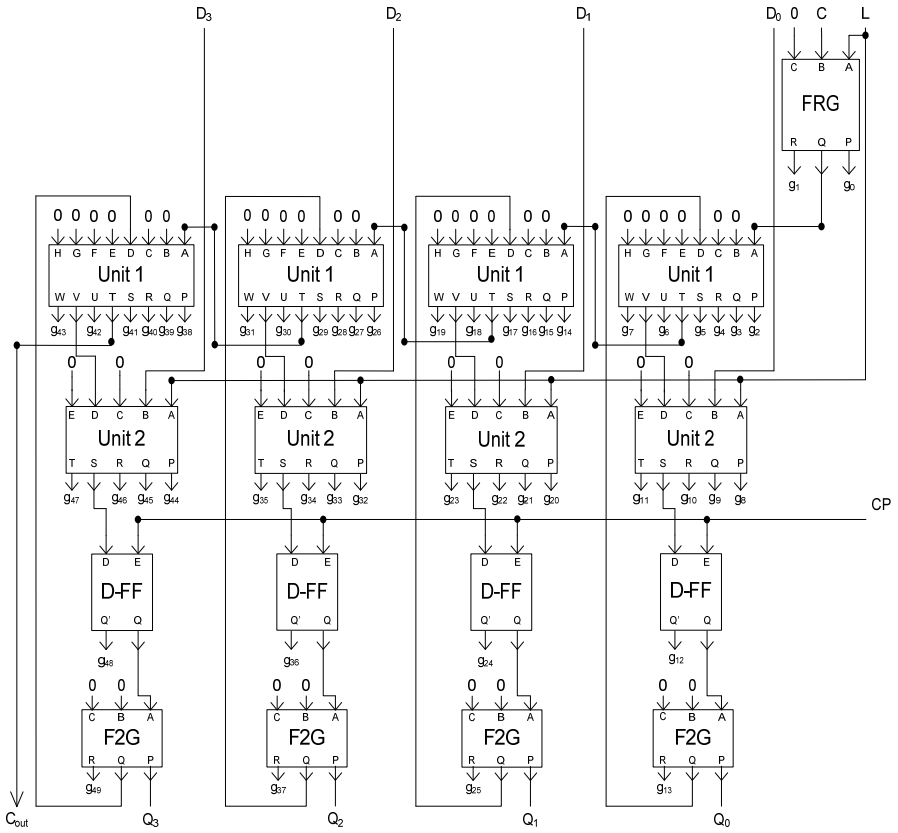


Fig. 17: First Approach of Fault Tolerant Reversible 4-Bit Binary Counter with Parallel Load

9. A Fault Tolerant Reversible 4-Bit Binary Counter with Parallel Load:

We propose the robust fault tolerant circuits for a 4-Bit binary counter with parallel load. These circuits are presented as three approaches. In this section, we will describe these approaches and will discuss about their features.

9.1. Approach 1: primary design of 4-Bit binary counter using Unit 1 and Unit 2 gates:

In this approach, the counter circuit is implemented using FRG, Unit 1, Unit 2, D-FF and F2G gates. This approach is a primary design of fault tolerant reversible 4-Bit counter. The functionality of this approach is depicted in Fig. 17. This is a first attempt of fault tolerant circuit for a 4-Bit binary counter. The number of the constant inputs, garbage outputs and Total quantum cost of its circuit is more than subsequent approaches. Nevertheless, this design has maximum number of Total logical calculation. In fact, this is a first layout of the proposed circuits. The evaluation of this approach is shown in Table 5.

9.2. Approach 2: implementing the counter circuit using Unit 3 gate:

In second approach, Unit 3 gate has been used instead of Unit 1 and Unit 2 gates. Total logical calculation of Unit 3 gate is lesser than those gates. Thus, Total logical calculation of this approach is better than previous approach. Minimum number of QC is the other future of this approach. Nevertheless, the number of constant inputs and garbage outputs is lesser than first approach. The functionality of this approach is shown in Fig. 18. This approach is an optimal state of 4-Bit binary counter. The number of constant inputs and garbage outputs of this circuit is more than subsequent approach. The evaluation of this approach is represented in Table 5.

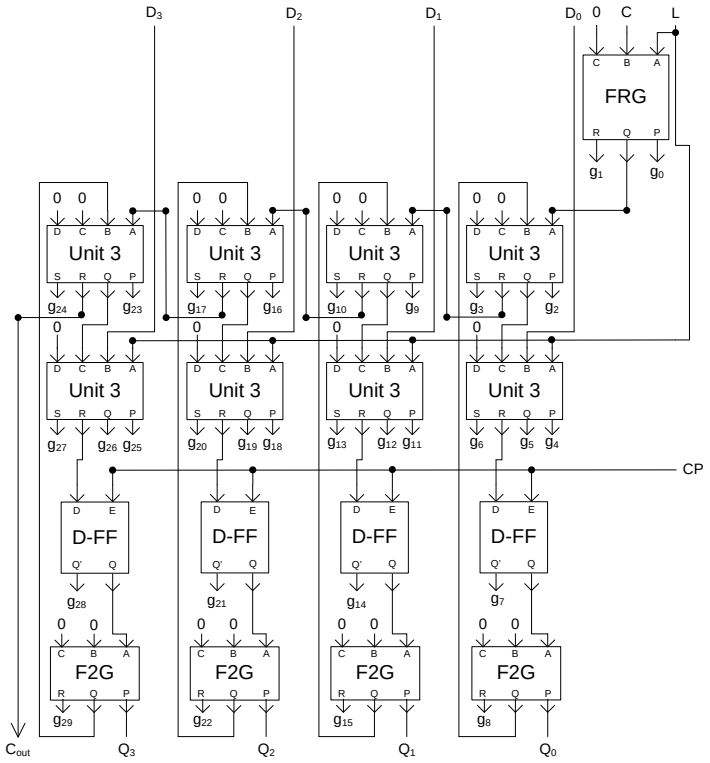


Fig. 18: Second Approach of Fault Tolerant Reversible 4-Bit Binary Counter with Parallel Load

9.3. Approach 3: Connecting Some Of The Garbage Outputs To The Unimportant Constant Inputsl

Finally, we propose an optimal design of this counter by connecting some of the garbage outputs to the unnecessary constant inputs. This approach is a robust and optimal circuit. Thus, it is better than the previous mentioned approaches. The number of used reversible gates and Total logical calculation in this approach is equal to previous approach. Connecting these garbage outputs to the unimportant inputs due to this circuit design has minimum number of constant inputs and garbage outputs. The capabilities of this method are shown in Fig. 19. This is a robust and optimal state of a 4-Bit binary counter with parallel load. The summarized evaluation of this circuit is shown in Table 5.

10. Evaluation of The Proposed Fault Tolerant Circuits:

The proposed fault tolerant reversible approaches are the robust and efficient circuits. They have some of the optimal and important factors like minimum constant inputs and garbage outputs. Evaluation of the proposed circuits is represented in Table 5.

The proposed approaches are not very sophisticated circuits. That is, we represented the mentioned proposed circuits easily.

The only difference between our variant approaches is using Unit 1 and Unit 2 gates in first approach, applying Unit 3 gate instead of these gates in second approach and reducing the garbage outputs and constant inputs in third approach. We are used Unit 3 gate instead of Unit 1 and Unit2 gates in second approach, because it has minimum number of constant inputs, garbage outputs, Total quantum cost and Total logical calculation.

In this section, we discuss about Total logical calculation of the proposed circuits and compare them together. In fact, the count of XOR, AND, NOT logic in the outputs are called Total logical calculation. We dedicate a symbol for the used calculation operations as:

α = A two input EX-OR gate calculation

β = A two input AND gate calculation

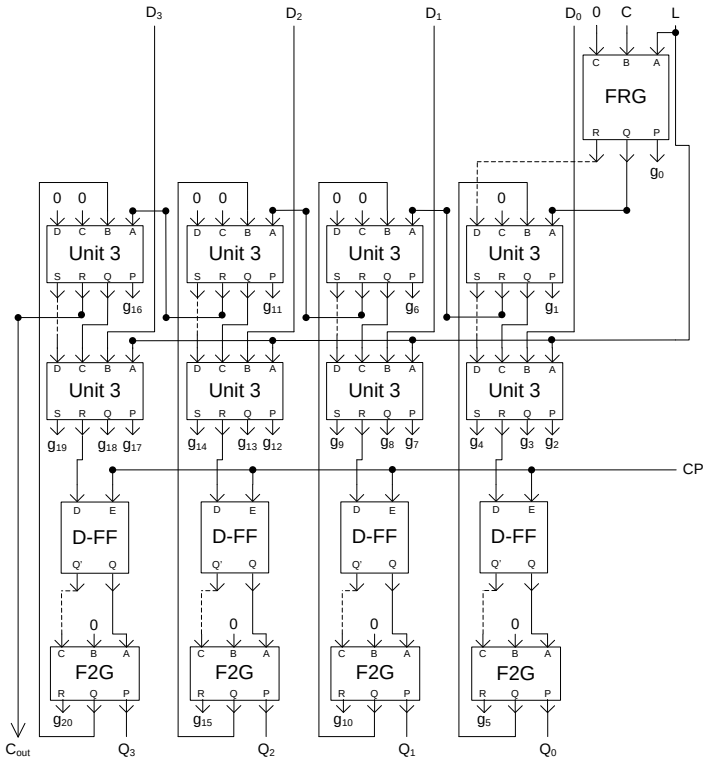


Fig. 19: Third Approach of Fault Tolerant Reversible 4-Bit Binary Counter with Parallel Load

δ = A NOT gate calculation
T = Total logical calculation

The FRG gate has two XOR, four AND plus two NOT operations in its output expressions. Therefore, Total logical calculation of this gate is as:

$$T_{(FRG)} = 2\alpha + 4\beta + 2\delta$$

The output expressions of F2G gate has two XOR operations that are formed its circuit design. Therefore, Total logical calculation of this gate is as:

$$T_{(F2G)} = 2\alpha$$

The Unit 1 gate calculates fourteen XOR, four AND plus two NOT in its output expressions. Thus, Total logical calculation of its circuit is as:

$$T_{(Unit\ 1)} = 14\alpha + 4\beta + 2\delta$$

The output expressions in the Unit 2 gate have six XOR, eight AND plus four NOT operations. Thus, Total logical calculation of the Unit 2 gate is as:

$$T_{(Unit\ 2)} = 6\alpha + 8\beta + 4\delta$$

The output expressions in the Unit 3 gate have four XOR, two AND plus one NOT operations. Therefore, Total logical calculation of the Unit 3 gate is as:

$$T_{(Unit\ 3)} = 4\alpha + 2\beta + 1\delta$$

Table 5: Comparative experimental results of the proposed fault tolerant reversible circuits

Approach #	No. of gates	No. of constant input	No. of garbage output	Total quantum cost	Total logic calculation
Approach 1	17	41	50	125	$122\alpha + 116\beta + 58\delta$
Approach 2	17	21	30	109	$74\alpha + 84\beta + 42\delta$
Approach 3	17	12	21	109	$74\alpha + 84\beta + 42\delta$

The Unit 4 gate have eight XOR, sixteen AND plus eight NOT operations in its output expressions. Thus, Total logical calculation of the Unit 4 gate is as:

$T_{(Unit\ 4)} = 8\alpha + 16\beta + 8\delta$

Total logical calculation of the D-FF gate is equal to Total logical calculation of the Unit 4 circuit. Therefore, Total logical calculation of its circuit is as:

$T_{(D\text{-}FF)} = 8\alpha + 16\beta + 8\delta$

In addition, The QC values of the applied gates in our proposed circuits are as:

$QC_{(FRG)} = 5$
$QC_{(F2G)} = 2$
$QC_{(Unit\ 1)} = 11$
$QC_{(Unit\ 2)} = 7$
$QC_{(Unit\ 3)} = 7$
$QC_{(Unit\ 4)} = 10$
$QC_{(D\text{-}FF)} = 10$

In approach 1, we are used one FRG, four Unit 1, four Unit 2, four D-FF and four F2G gates. It is initial design of the proposed fault tolerant reversible circuits. The number of Total quantum cost and Total logical calculation in this approach is computed as:

$QC_{(Approach\ 1)} = (QC_{(FRG)} * 1) + (QC_{(Unit\ 1)} * 4) + (QC_{(Unit\ 2)} * 4) + (QC_{(D\text{-}FF)} * 4) + (QC_{(F2G)} * 4) = (5 * 1) + (11 * 4) + (7 * 4) + (10 * 4) + (2 * 4) = 5 + 44 + 28 + 40 + 8 = 125$

$T_{(Approach\ 1)} = (T_{(FRG)} * 1) + (T_{(Unit\ 1)} * 4) + (T_{(Unit\ 2)} * 4) + (T_{(D\text{-}FF)} * 4) + (T_{(F2G)} * 4) = (2\alpha + 4\beta + 2\delta) + (56\alpha + 16\beta + 8\delta) + (24\alpha + 32\beta + 16\delta) + (32\alpha + 64\beta + 32\delta) + (8\alpha) = 122\alpha + 116\beta + 58\delta$

The proposed circuit in approach 2 is designed using one FRG, eight Unit 3, four D-FF and four F2G gates. It is second state of the proposed fault tolerant reversible counter. The number of Total quantum cost and Total logical calculation in its circuit is calculated as:

$QC_{(Approach\ 2)} = (QC_{(FRG)} * 1) + (QC_{(Unit\ 3)} * 8) + (QC_{(D\text{-}FF)} * 4) + (QC_{(F2G)} * 4) = (5 * 1) + (7 * 8) + (10 * 4) + (2 * 4) = 5 + 56 + 40 + 8 = 109$

$T_{(Approach\ 2)} = (T_{(FRG)} * 1) + (T_{(Unit\ 3)} * 8) + (T_{(D\text{-}FF)} * 4) + (T_{(F2G)} * 4) = (2\alpha + 4\beta + 2\delta) + (32\alpha + 16\beta + 8\delta) + (32\alpha + 64\beta + 32\delta) + (8\alpha) = 74\alpha + 84\beta + 42\delta$

Total quantum cost and Total logical calculation of approach 3 is like approach 2, because only difference factor between them is number of the constant inputs and garbage outputs. Therefore, Total quantum cost and Total logical calculation of this approach are as:

$QC_{(Approach\ 3)} = 109$
$T_{(Approach\ 3)} = 74\alpha + 84\beta + 42\delta$

The mentioned approaches of the proposed counter circuits have same number of the reversible gates, because we only are used some of the important factors like Total logical calculation and Total quantum cost. Thus, the number of their reversible gates is equal together.

One of the main factors in the reversible circuit logic is number of the constant inputs. These inputs are added to an n×k function to generate its circuit as a reversible logic state. Some of the constant inputs are not required to special value. That is, amount of them can be as '0' or '1' bit. But, some of them have to be a special bit number. For example, when we use the Unit 1 gate for AND operation, one of the input bits (H) can be '0' or '1' signal and it does not require to unique signal value. Approach 1 has 41 constant inputs and approach 2 has 21 constant inputs, but the number of constant inputs in approach 3 is 12. The reason of existence the reduced constant inputs in approach 3 is connecting some of the garbage outputs to the unimportant constant inputs.

Garbage outputs are some of the outputs that are not important outputs in the reversible circuits. We can connect some of these outputs to the unimportant constant inputs to reduce QC of the desired circuit. In our proposed circuits, approach 1 has 50 garbage outputs and approach 2 has 30 garbage outputs, while number of the garbage outputs in approach 3 is 21, because some of them are connected to the unnecessary constant inputs. Thus, approach 3 present optimal and robust fault tolerant circuit of the mentioned counter. That is, it is better than both of the approach 1 and approach 2.

One of the major factors in the reversible logic circuit is Total quantum cost. It is other important factor of the reversible circuit logic. Total quantum cost of the proposed first approach is 125, but Total quantum cost of the subsequent approaches is 109, because we are designed their circuits using Unit 3 gates. Thus, we have to compare the proposed approaches by other factors like number of gates, constant inputs and etc.

Based on the mentioned factors, we can summarize that our approaches are new efficient and robust circuits of the fault tolerant reversible 4-Bit binary counter with parallel load, although approach 3 is better than the prior proposed approaches. This subject is demonstrated by comparing their circuits and represented results in Table 5.

Conclusion:

In this paper, we proposed the fault tolerant reversible circuits of 4-Bit binary counter with parallel load. They are the robust and optimal states of the mentioned counter. We presented the proposed circuits by three approaches. All approaches have efficient features, but approach 3 is implemented by the better methods. We reduced number of the reversible gates, constant inputs and garbage outputs in the mentioned approaches. Table 5 demonstrates results of the proposed circuits. Some of the complex circuits would be implemented using our proposed fault tolerant circuits in the future.

According to the discussed contents, we can contend and summarize that our proposed approaches are the robust and efficient circuits of this counter. All the circuits have nanometric scales.

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